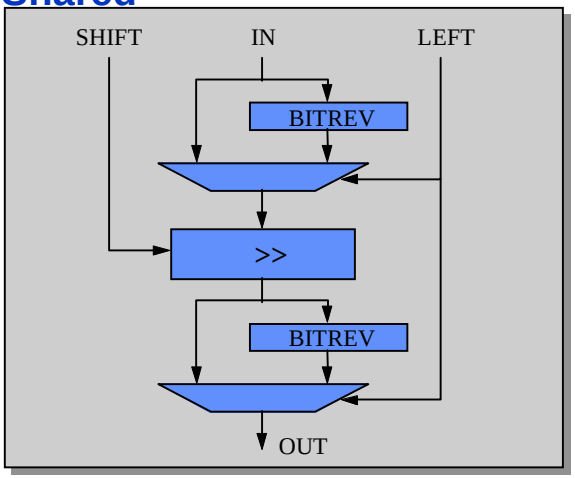
Architectural Trade-Offs

Conceptual View

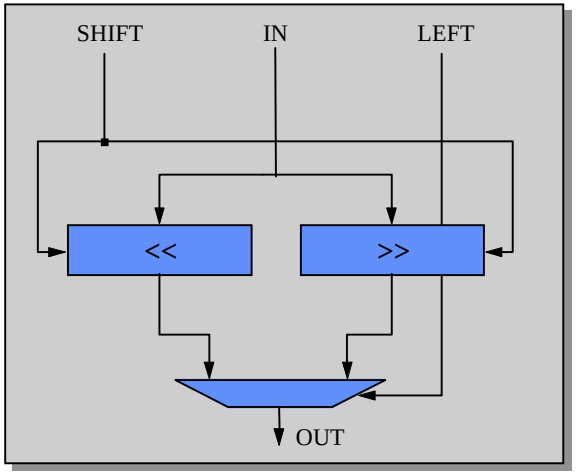
Module Compiler Code

Shared



XIN = LEFT ? bitrev(IN) : IN;
XOUT = XIN >> SHIFT;
OUT = LEFT ? bitrev(XOUT) : XOUT;

Parallel



wire [width] z_left = a<<shift;
wire [width] z_right = a>>shift;
z = left ? z_left : z_right ;

	Area (gates)	Delay (ns)	RT (min)	Comments
Shared	258	2.05	< 1	32-bit data, 5-bit shift
Parallel	398	1.86	< 1	32-bit data, 5-bit shift

Using .25u, 3.3V process, worst-case operating condition

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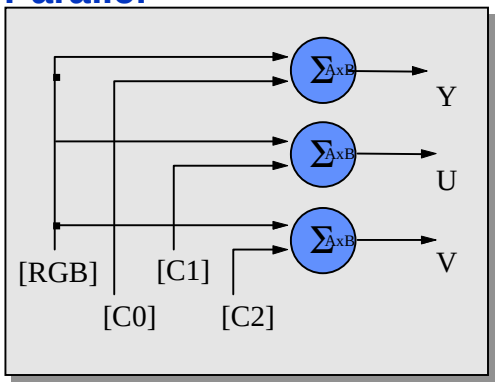
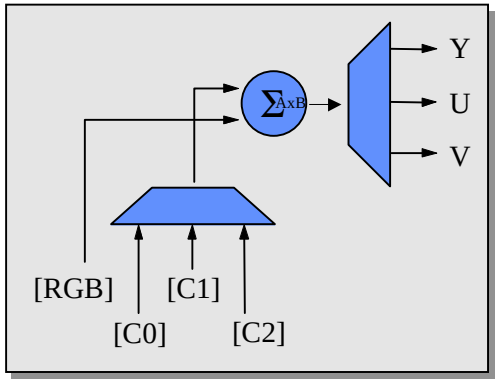
Parallel



*Y = C00*R + C01*G + C02*B;*
*U = C10*R + C11*G + C12*B*
*V = C20*R + C21*G + C22*B*

Serial



C0 = SEL ? C00 : C10 : C20;
C1 = SEL ? C01 : C11 : C21;
C2 = SEL ? C02 : C12 : C22;
*YUV = C0*R + C1*G + C2*B;*
demux(YUV, SEL, Y, U, V);

	Area (gates)	Delay (ns)	RT (min)	Comments
Parallel	589	3.19	< 1	8-bit data; constant coeffs
Serial	986	5.05	< 1	8-bit data; constant coeffs
Parallel	2356	4.66	< 1	8-bit data; **variable** coeffs

Using .25u, 3.3V process, worst-case operating condition